iJETRM
International Journal of Engineering Technology Research & Management

IMPLEMENTATION OF VOLTAGE CONTROLLED OSCILLATOR WITH DISCRETE AND CONTINUOUS TUNING CIRCUIT

PragnaGalagli, Sanjana V Ghate,Shabarish Babu B V
Ravish Aradhya H.V, Usha Rani K.R, Sahana B
Electronics and Communication Department, R.V College of Engineering, Bengaluru, India
pragnagalgali@gmail.com
ghatesanjana@gmail.com
shabarishbabubv@gmail.com
ravisharadhya@rvce.edu.in
usharani@rvce.edu.in
sahanab@rvce.edu.in

ABSTRACT
In the proposed work, a deterministic simulation-based approach is employed to achieve stable frequency of 5GHz, 10GHz and 50GHz. The design for the approach has been implemented using 45nm Standard CMOS technology. Even though there are plenty of research publications in this area, the design proposed in the following brief has both discrete and continuous tuning circuits that can operate at a lower power compared to the existing designs. Cross coupled configuration of the oscillator along with the buffer circuit is designed and simulated in Cadence Virtuoso. In depth Periodic Steady State Analysis along with Phase Noise analysis is carried out and the results are recorded.

KEYWORDS:
Voltage Controlled Oscillator, tuning circuits, buffers, phase noise, harmonic frequency

INTRODUCTION

The Voltage controlled oscillator can be classified into two types, 1. Waveform oscillator 2. Resonant oscillator. Waveform oscillator consists of ring oscillator topology and relaxation oscillator which has poor noise phase performance. Ring oscillator consists of LC tank oscillator topology and crystal oscillator which is neither integrated nor tunable. Few of the ideal VCO specifications are low noise, low power, integrated, have wide tuning range, small die area and have high operating frequency (GHz).

LC VCO has an outstanding phase noise and degrades performance due to jitter at high frequency. But it has a few disadvantages such as high-power consumption, occupation of a relatively large die area (since it contains inductor and varactor which require large area).With low power supply voltages, the tuning range of the monolithic LC voltage-controlled oscillator is limited [1]. “To incorporate such techniques, a 1.8GHz CMOS oscillator achieves a tuning range of 120MHz with relatively constant gain with a phase noise of -100dBc/Hz at 500MHz offset”. The actual design implementation is a quadrature generator which consists of two coupled oscillators. In the above-mentioned design, the performance parameters are achieved at 2.3 mA/oscillation supply current and 3.3 V supply voltage at 0.6um standard CMOS technology.To optimize and automate component and transistor sizing of CMOS LC oscillator, it is observed that performance measures can be formulated by posynomial functions of the design variable.

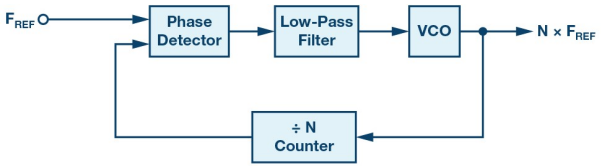

Fig. 1. Block Diagram of Phase Locked Loop System

iJETRM
International Journal of Engineering Technology Research & Management

Technology in communication demands transmitting and receiving data at high speeds and maintaining low errors rate. The communication systems are nothing but the composure of transmitter receiver and transceiver in top level overview as shown in Fig 1. All the activities are synchronized with the clocks and we cannot have more than 2 externals clocks to suffice different operating frequency requirements of different components of the system. To satisfy this requirement, phase locked loops are used as frequency synthesizers to generate the frequencies. These frequency synthesizers are used to generate LO signal which is used in mixes to demodulate the incoming signal in receivers. VCO with low phase noise is as much important as that of the presence of VCO because, undesirable phase noise makes the presence of a VCO unworthy. Along with the consideration of low power consumption of a VCO, low phase noise is the performance parameter is presented in this paper. The PLL consists of a phase frequency detector, charge pump, low pass filter and a voltage-controlled oscillator. Locking of PLL refers to equality in phase as well as frequency of incoming signal Fref and the signal from the output of divide by N counter. PFD detects the difference between Fref and feedback signal and generates a positive signal if Fref leads or negative signal when Fref lags. According to these positive or negative signals charge pump drivers or extracts current from low pass filter respectively. LPF will provide the according voltage to driver the OSC [1]. Phase noise of this VCO determines how clean the signal generated without any phase corruptions. Since Ring oscillators provide higher spectral purity with high Q factor, the sensitivity of the oscillators is very high. But the only drawback is that power consumption is an issue in RO. This can be solved by using active load concept [2]. This paper presents the simulated results with low phase noise value and proposes a circuit to realize low phase noise as well as power dissipation.

MOTIVATION

Voltage Controlled Oscillator, being the heart of modern communication system need to be optimized in all the aspects such as size, cost, power, speed, and stability of the frequency event at the highest possible range of frequency, which can be seen as an efficient design with upcoming technologies such as 5G. The design proposed in this paper focuses on the power and speed aspects, satisfying the requirement as mentioned previously.

PROBLEM STATEMENT

Design a low power and less jitter voltage-controlled oscillator with buffers along with discrete and continuous tuning circuits using 45 nm Standard CMOS Technology.

IMPLEMENTATION OF VOLTAGE CONTROLLED OSCILLATOR DESIGN

The schematic of cross coupled oscillator is as shown in figure 2. This cross coupled architecture has advantages over other type of implementation such as ring oscillator, RC feedback oscillator and many others. Ring oscillator even though it can produce frequencies of higher order, have large jitter and area consumption when compared to a cross coupled oscillator.

iJETRM
International Journal of Engineering Technology Research & Management

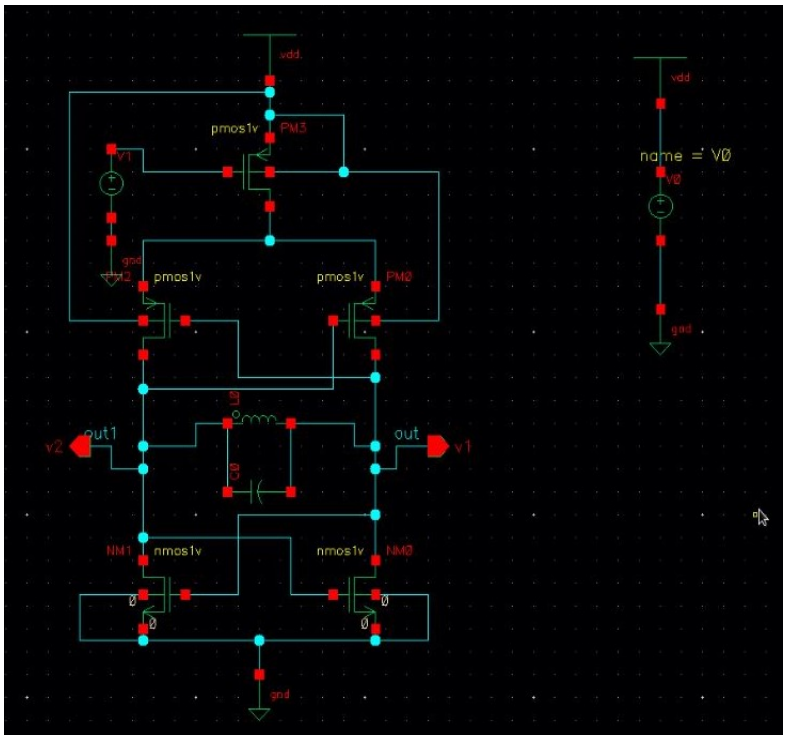

Fig. 2. Oscillator Schematic

The pmos1v at the top of the schematic below Vdd acts as the current source and the current is divided in 2 paths further downstream. The mosfet acting as the current source is biased in saturation region and the rest of the mosfets are biased accordingly, as shown in Table 1.

Table 1. DC Operating Points of the MOS transistors

Parameter	Pmos (Current Source)	Pmos (Cross Coupled)	Nmos (Cross Coupled)
Id (10^{-6} A)	105.03	52.5013	52.5013
gm ($10^{-6}Av^{-2}$)	53.7761	97.2198	143.189

The plots of the frequencies simulated are shown in figure 3 to figure 5 for different frequencies respectively.The settling time variation in case of all the 3 different frequencies can be observed where the signal is observed to be settling much faster at higher frequency of 50 GHz when compared to other 2 lower frequencies.

In figure 6. We can see the waveform of stabilized signal where the circuit is fully balanced with Barkhousen criteria defined for an oscillator to produce oscillations.

iJETRM
International Journal of Engineering Technology Research & Management

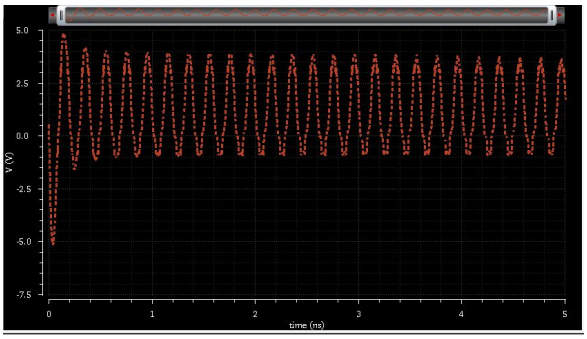

Fig. 3. Oscillations at 5GHz Frequency

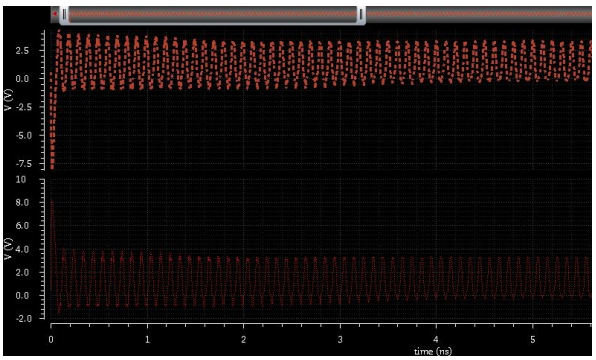

Fig. 4. Oscillations at 10GHz Frequency

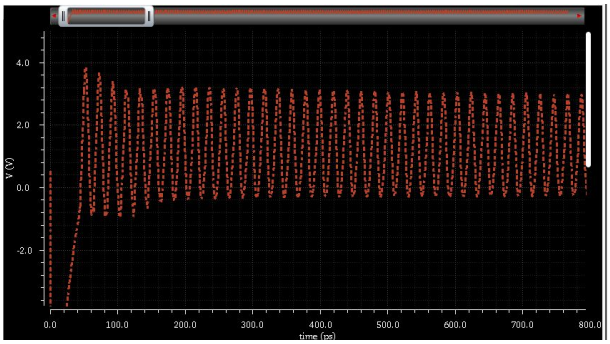

Fig. 5. Oscillations at 50GHz Frequency

iJETRM
International Journal of Engineering Technology Research & Management

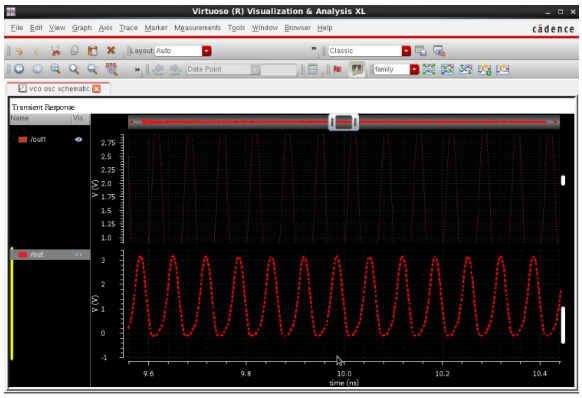

Fig. 6. Stabilized Oscillations at 15GHz Frequency

All the above oscillation frequencies are measusred using calculator tool and are being compared with the frequency measured from the 1st harmonic frequency of periodic dteady state analysis in Table 2.

Table 2. Comparison Table for Operating Frequencies

Oscillator frequency (GHz)	Frequency from Calculator (GHz)	1st Harmonic Frequency (PSS Analysis) (GHz)
5	5.01	4.99
10	9.966	9.99
15	14.96	15.001
50	48.98	49.35

Table 3. Specification Table for Inductor and Capacitor

Oscillator frequency	Inductor Value	Capacitor Value	Peak to Peak Voltage
5GHz	1nH	1.0132pF	4.301v
10GHz	1nH	0.2533pF	3.517v
15GHz	1nH	112fF	3.41v
50GHz	1nH	10.132fF	3.445v

From all the data, it could be interpreted that as we operate at higher frequencies, peak to peak amplitude is reducing gradually, this need to be addressed with buffers and tuning circuits that could be placed at the outputs.

iJETRM
International Journal of Engineering Technology Research & Management

Figure 7. shows that phase noise analysis plot at 10GHz frequency. It could be extrapolated that around 109Hz the phase noise is expected to be at least -175 dBc/Hz. This value of phase noise is extremely good enough to engage the specifications of modern communication technologies.

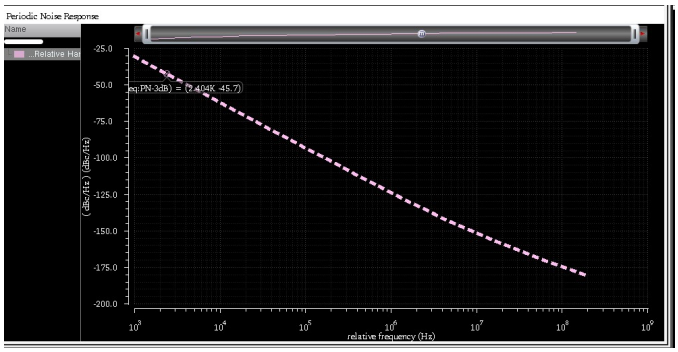

Fig. 7. Phase Noise Plot at 15GHz Frequency

Voltage controlled oscillator is an improved version of normal cross coupled oscillator. This comes with the continuous and discrete tuning circuits along with the buffers to avoid amplitude compression at the output.

VCOs generally suffer from issues such as supply pushing, phase noise, load pulling and effects of radiated energy from neighboring amplifiers. In case of frequency pulling, when an interferer's amplitude at the VCO output port is sufficient, it can cause the VCO to shift its oscillation frequency to match with the interfering frequency. These effects can induce voltage changes and result to degrade the performance of the oscillator. The RF energy conduction along the signal path and back to VCO output can also cause the issues mentioned above. The most common design practice to prevent all these problems from affecting the design oscillators is to provide isolation using buffers which is shown in figure 8.

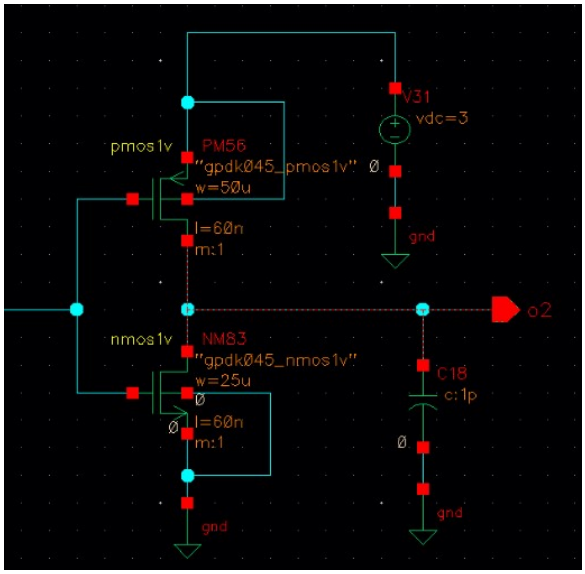

Fig. 8. Buffer Circuit

iJETRM
International Journal of Engineering Technology Research & Management

The buffer parameters are recorded in Table 4.

Table 4. Buffer Parameters

Vdd	3v
Pmos	
W	50um
L	60nm
Nmos	
W	25um
L	60nm
Capacitance	1pF

The oscillators that employ tuning circuits are called tuned oscillators, wherein the tuning circuits are constructed using inductors and/or capacitors. The tuning circuits generally perform two types of tuning – Discrete, also called as fine tuning and continuous, also called as coarse tuning. Fixed frequencies are achieved using capacitors. Tuning circuits are used to convert the fixed frequency oscillators into VCOs through replacement of tuning capacitors by varactor diode.

Coarse tuning is achieved using a varactor diode. A varactor can be modelled as a variable capacitor in series with a resistance as seen in figure 9. The capacitance of the varactor depends on the junction area, the reverse bias voltage and density of doping of the semiconducting material. The value of the varactor is varied in order to achieve relatively larger changes in the resulting signal frequencies. The fine tuning in is achieved through varactor blocks which provide precise operating frequency. The varactor blocks of consist of multi – fingered varactors which are parallelly connected to maximize the tunability of the VCO. The parameters of course tuning circuit is recorded in Table 5.

Discrete tuning is achieved through a capacitor array bank. The discrete tuning in is achieved through a switched capacitor array block that has parallelly connected capacitor blocks that can be switched on or off, depending on the capacitance requirement as seen in figure 10. The capacitor array bank and VCO switches in [1] are realized and implemented using NMOS and PMOS transistors or capacitors. The parameters of discrete tuning circuit are recorded in Table 6.

Table 5. Varcap Parameters

Capacitance	4.99fF
Multiplier value to vary capacitance	5
Total C	25fF

The value of multiplier is changed in order to change the capacitance value of varcap. Cap Bank shown in fig. 10. is simulated with Vdd 3v and R value 21kΩ.

iJETRM
International Journal of Engineering Technology Research & Management

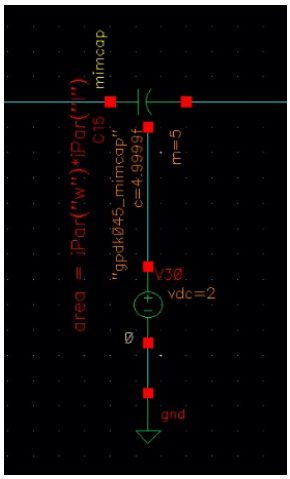

Fig. 9. Continuous Tuning Circuit

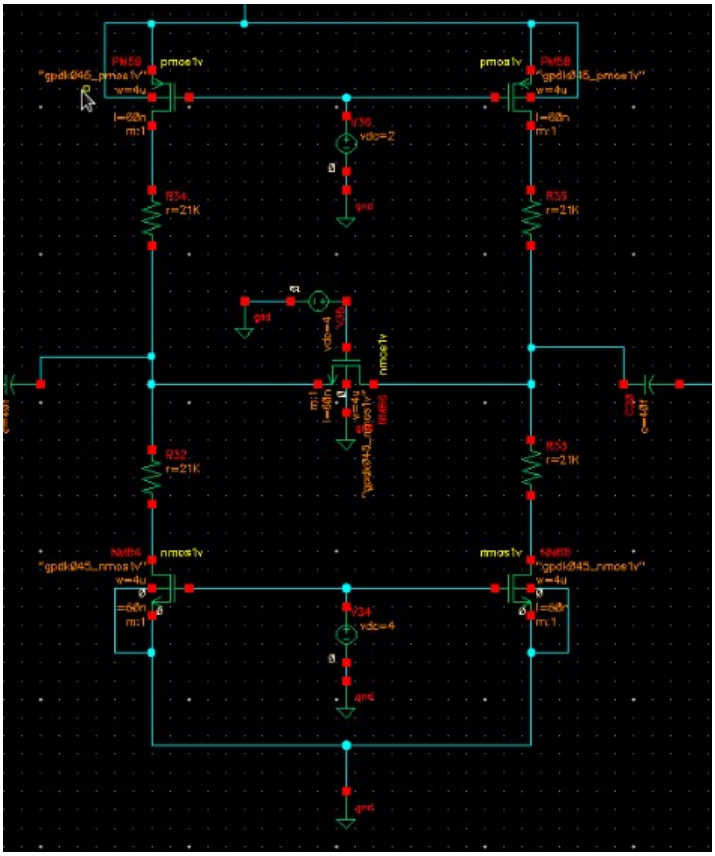

Fig. 10. Discrete Tuning Circuit Cap Bank Schematic

iJETRM
International Journal of Engineering Technology Research & Management

Table 6. Parameters of Cap Bank Circuit Components

Parameters	Pmos	Nmos
W, L (m)	4u, 60n	4u, 60n
Bias Voltage in On Condition (V)	4	0
Bias Voltage in Off Condition (V)	2	4

After addition of all the above assisting circuits the Voltage controlled oscillator is simulated at 5GHz operating frequency as sown in figure 10. Frequency can be varied in the range of kHz using different logical combinations such as 0011, 1100 or even an 8 bit discrete tuning can be done according to the area constraint. Similarly the voltage for varcap is directly proportional to the oscillating frequency. Hence Variation in Ghz range can be done using continuous tuning option.

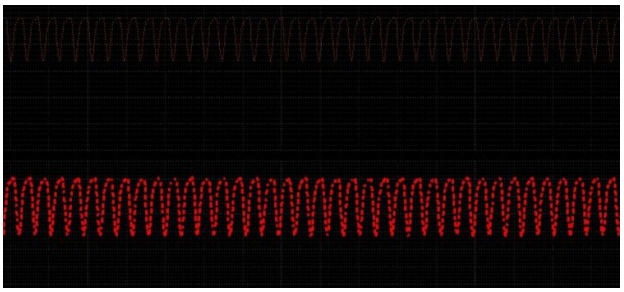

Fig. 11. Resulting Oscillation

CONCLUSION

By addition of circuits such as tuning and buffer circuits with the above-mentioned parameter values, the phase noise, jitter time and amplitude compression issues are reduced to maximum extent at the cost of area in the design.

REFERENCES

[1] B. Razavi, "A 1.8 GHz CMOS voltage-controlled oscillator," 1997 IEEE International Solids-State Circuits Conference. Digest of Technical Papers, San Francisco, CA, USA, 1997, pp. 388-389.W.-K. Chen, Linear Networks and Systems (Book style). Belmont, CA: Wadsworth, 1993, pp. 123–135.

[2] W. De Cock and M. Steyaert, "A CMOS 10GHz voltage-controlled LC-oscillator with integrated high-Q inductor," Proceedings of the 27th European Solid-State Circuits Conference, Villach, Austria, 2001, pp. 498-501.

[3] P. Gupta and M. Kumar, "Power efficient voltage-controlled oscillator design in 180nm CMOS technology," 2017 International Conference on Computing, Communication and Automation (ICCCA), Greater Noida, 2017, pp. 1470-1476.

[4] M. D. M. Hershenson, A. Hajimiri, S. S. Mohan, S. P. Boyd and T. H. Lee, "Design and optimization of LC oscillators," 1999 IEEE/ACM International Conference on Computer-Aided Design. Digest of

iJETRM
International Journal of Engineering Technology Research & Management

Technical Papers (Cat. No.99CH37051), San Jose, CA, USA, 1999, pp. 65-69.B. Smith, “An approach to graphs of linear forms (Unpublished work style),” unpublished.

[5] N. Retdian, S. Takagi and N. Fujii, "Voltage controlled ring oscillator with wide tuning range and fast voltage swing," Proceedings. IEEE Asia-Pacific Conference on ASIC,, Taipei, Taiwan, 2002, pp. 201-204.

[6] A. Kushnerov and A. Yakovlev, "Stacking voltage-controlled oscillators: Analysis and application," 2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS), Monte Carlo, 2016, pp. 53-56.

[7] P. Dudulwar, K. Shah, H. Le and J. Singh, "Design And Analysis Of Low Power Low Phase Noise VCO," Proceedings of the International Conference Mixed Design of Integrated Circuits and System, 2006. MIXDES 2006., Gdynia, 2006, pp. 256-259.

[8] V. V. Ulansky and H. M. Elsherif, "A voltage-controlled oscillator based on negative inductance converter," 2015 IEEE 35th International Conference on Electronics and Nanotechnology (ELNANO), Kiev, 2015, pp. 508-511.

[9] Zhang Jianhui, Lu Tiejun and Xia Zenglang, "Study of CMOS voltage-controlled oscillator design," Proceedings of 2005 IEEE International Workshop on VLSI Design and Video Technology, 2005., Suzhou, China, 2005, pp. 59-62.

[10] A. Jha, K. Liao, G. Yeap and K. O. Kenneth, "Voltage controlled oscillator area reduction in nano-scale CMOS," 2014 IEEE Radio Frequency Integrated Circuits Symposium, Tampa, FL, 2014, pp. 421-424.

[11] I. Ghorbel, F. Haddad and W. Rahajandraibe, "Optimization of voltage-controlled oscillator VCO using current-reuse technique," 2014 26th International Conference on Microelectronics (ICM), Doha, 2014, pp. 212-215.

[12] Nguyen Phuong Thi Le, K. T. Low and Libin Yao, "High linearity voltage-controlled oscillator," 2009 IEEE 8th International Conference on ASIC, Changsha, Hunan, 2009, pp. 363-366.

[13] J. Garg and S. Verma, "Design of low power Voltage Controlled Oscillator," 2012 1st International Conference on Emerging Technology Trends in Electronics, Communication & Networking, Gujarat, 2012, pp. 1-4.

[14] V. Macaitis and R. Navickas, "CMOS technologybased LC VCO review," 2015 Open Conference of Electrical, Electronic and Information Sciences (eStream), Vilnius, 2015, pp. 1-4.

[15] A.Allam, I.M Filanovsky, “Synchronization of Mutually coupled LC-Oscillator.

[16] https://www.analog.com/en/analog-dialogue/articles/phase-locked-loop-pll-fundamentals.html#