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A SURVEY ON DIFFERENT ADIABATIC LOGIC CIRCUITS FOR LOW POWER IN DSM TECHNOLOGY

Mohd. Farid Khan[*1]
Uday Panwar[2]
[*1,2]Dept. Electronics & Communication Engg. SIRT, Bhopal, 462051, India
Farid.khan85@gmail.com
panwaruday1@gmail.com

ABSTRACT
In last few years power dissipation is one of the main problems of VLSI circuit design, for which CMOS is the technology which is highly used due to the ever growing demand for portable and small sized devices, mobile applications. These electronic gadgets require logic circuit design methods to realize integrated circuits with less power dissipation. Even before the mobile age, power dissipation has been a central problem. To solve the problem of power dissipation, many researchers have put forward different ideas from the device level to the architectural level and above. But as we are moving into the era of Ultra Low power applications we need designs that are even more power efficient. Also it is required to keep the transistor count at minimum. This paper investigates different adiabatic logic families such as ECRL, 2N-2N2P and PFAL. All simulations are carried out using HSPICE at 65nm technology with supply voltage is 1V at 100MHz frequency, for fair comparison of results W/L ratio of all the circuit is same. Finally average power dissipation characteristics are plotted with the help of a graph and comparisons are made between different logic families

Keywords:
Low power, Adiabatic logic, ECRL, 2N-2N2P, PFAL

INTRODUCTION

If we want to design a circuit for low power dissipation application then it is important to have a deep understanding of the sources of power dissipation, the factors which influence them, the methodologies and techniques that are available to achieve optimal results. Therefore, my dissertation starts with the sources of power dissipation. Power consumption comprises of two parts: dynamic power and static power. The dynamic power loss occurs to the switching activities during charging and discharging process, while static power is caused due to the device internal leakage when the circuit is in the idle state. Therefore, we need to consider both dynamic power and static power in the low-power VLSI circuit design. Low-power design can be applied on different levels, such as the architectural level, the gate level, and the technology level. A lot of efficient circuit technologies like sub-threshold circuit [1-3].

Low-power design can be applied on different levels, such as the architectural level, the gate level, and the technology level. A lot of efficient circuit technologies like sub-threshold circuit [4] and multi-threshold technology [5-6] have been introduced to reduce dynamic power. Losses occurring because of leakage currents are in focus with on-going shrinking of electronic circuits. Power-gating does not supply power to the circuits in off state from the power supply. Non-critical paths within a complex system can be paired with higher V_{th} devices, resulting in a compromise of speed for passive losses. Apart from these circuit level methods to reduce leakage losses also new transistor models are presented to minimize leakage losses in circuits [7-9].

Adiabatic Logic technique is one of the most efficient circuit design methods to reduce energy consumption in different operations. Study of adiabatic logic on the gate level suggests a major reduction of losses compared to static CMOS. Adiabatic logic utilizes AC voltage supply rather than DC voltage supply to recycle the energy of circuits. This method forces the node voltage to vary synchronously with the power supply; as a result, the energy stored in the node capacitance is only $0.5CV_{DD}^2$, which avoids the heat dissipation in charging and discharging period. Furthermore, the energy stored can flow back to the voltage supply when the supply recovers to zero. Theoretically, zero power consumption can be realized by the adiabatic logic without considering the leakage power. Circuit simulation is carried out using Cadence Virtuoso at 65nm technology [10-15].

In this paper, power dissipation is calculated for different logic gates using different adiabatic logic circuits and results are compared to see the effectiveness of different adiabatic logic families as compared to conventional

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CMOS circuits.The rest of the paper is organized as follows: Section 2 overviews the conventional CMOS and adiabatic logic circuits.In section 3, simulation of circuits is done and results of power dissipation are compared. The paper ends with the conclusion given in section 4.

Conventional CMOS and ADIABATIC LOGIC

Manash Chanda et al.propose implementation of subthreshold Adiabatic Logic for Ultralow-Power Application, in this paper author has analysed the performance of logic circuits in subthreshold region to make improvements for Ultra Low power applications. The efficiency of subthrehold adiabatic logic has been has been presented by designing and simulating a 4 bit CLA. Sonal Aron et. atdescribed the method of decreasing the peak power dissipation of the mux. It is concluded that the peak power dissipation is decreased by 29.876 microwatts by employing the PFAL adiabatic technique in the implementation of MUX. In fact, this decrease in power dissipation can proves to be very advantageous for low power, Sowmiya.M1 et.proposed basic gates using PFAL adiabatic logic circuits. The author found that the proposed adiabatic logic circuit is advantageous to ultra- low power applications as result showed that NOT gate, NOR gate and NAND gate achieved power reduction of 23%, 36.1% and 42.8% respectively compared to conventional CMOS logic gates using Tanner EDA. Also among three gates, NAND gate consume less power and proves that positive feedback adiabatic logic based NAND gate can be used for ultra-low power circuits, VijendraPratap Singh et. atdiscussed about the drawback of PFAL. It is concluded that although the adiabatic PFAL offers significant power reduction and so better power performance over conventional static CMOS but suffers from large switching time, so it is not suitable for application where the delay is critical. Thus, suffers from low speed of operation and is not suitable for the application where fast switching is required.V. S. KanchanaBhaaskaranproposesEnergy Recovery Performance of Quasi-Adiabatic Circuits using Lower Technology Nodes, author presentsthe modeling and performance efficiency analysis of the sense-amplifier based quasi-adiabatic structures, namely, the 2N-2P, 2N-2N2P, PFAL and the DCPAL circuits. This work sheds light on the effect of charging/discharging path resistance of the circuits, the dissipation due to current leakage paths and floating nodes, effect of the circuit structure on the adiabatic frequency range and the comparative advantage of the pre-resolving capability of the DCPAL structure.

Adiabatic LOGIC

The use of AC power clock as opposed to DC supply makes the adiabatic circuits capable of recovering the stored energy of node capacitors back to the power source, and hence, avoid the dynamic power loss almost completely, theoretically. The use of adiabatic logic principle in designing of low power circuits, is continuously growing, and is proving to be a better selection in comparison to other conventional circuits [Fig. 1]. In the WAIT phase the power clock stays at low (zero) value, which maintains the outputs at low value, and the evaluation logic generates pre-evaluated results. Now, since the power clock is at low level, the pre-evaluated inputs will not affect the state of the gate. In the EVALUATE phase, the power supply ramps up from zero to Vdd gradually, and the outputs will be evaluated as per the result of pre-evaluation logic. In the HOLD phase, power clock stays high, providing the constant input signal for the next stage in pipelining of adiabatic circuits, and keep the outputs valid for the entire phase. Meanwhile inputs ramp down to low value. In the RECOVERY phase of operation, the power supply ramps down to zero and the energy of the circuit nodes is recovered back to the power source instead of being dissipated as heat [12].

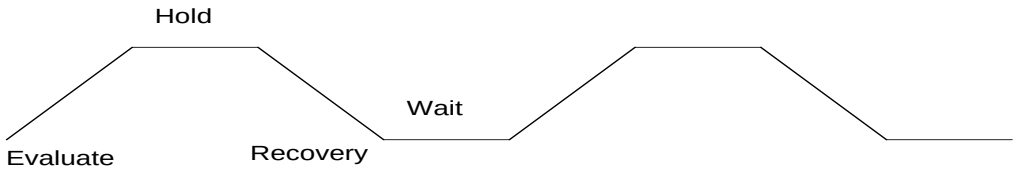

Fig.1: Four Phased Trapezoidal Power Clock

EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

Efficient Charge Recovery Logic (ECRL) [5], as shown in Fig. 2, uses two cross-coupled PMOS transistors and two NMOS transistors in the N-functional blocks of ECRL logic block. In order to recover and reutilize the supplied energy, ECRL gates uses AC power clock (pck). Let us assume **In**is at high and **Inb** is at low. At the beginning of a cycle, when power clock 'pck' rises from zero to VDD, **Out** remains at low level because the

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high input **In** turns the F NMOS logic high. Output **Outb**follows the power clock 'pck' through M1. Now when 'pck' reaches to VDD, the outputs hold valid logic values. During the hold phase these output values are maintained and can be used as inputs for evaluation of next stage. In the next phase of recovery, the power clock falls down to zero level and the energy from the output node can be returned to the 'pck' so as to recover the delivered charge [13-16].

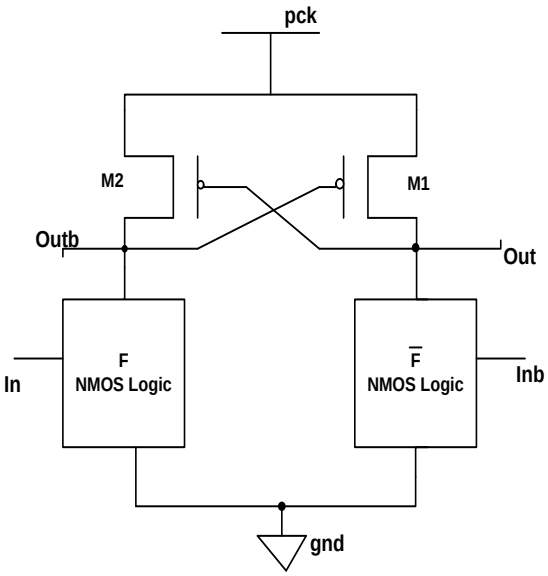

Fig.2: Efficient Charge Recovery Logic (ECRL)

2N-2N2P LOGIC

The 2N-2N2P is a quasi-adiabatic logic circuit. NMOS transistors are used for non-floating output and PMOS transistors are used for pre charge and recovery path. Figure 3 shows the 2N-2N2P inverter which consists of a cross coupled latch formed by MN1-MP1 and MN2-MP2 inverter circuits MN3 and MN4 constitute the logic functional block that are connected in the pull down network. These functional blocks can be replaced by any other desired logic for creating the required stage in the adiabatic pipeline [22] The energy recovery operation is similar to 2N2P logic but its additional advantage is to prevent floating output node when neither MP1 nor MN1 conducts with respect to /OUT node, or when neither MP2 nor MN2 conducts with respect to OUT node.[10, 17-19].

POSITIVE FEEDBACK ADIABATIC LOGIC (PFAL)

The Positive Feedback Adiabatic Logic (PFAL) achieves the lowest power consumption as opposed to other similar adiabatic logic families. The generalized PFAL circuit diagram is shown in Fig.4. The latch is made similar to the 2N-2N2P logic circuit with two PMOS transistors and two NMOS transistors. The functional blocks of NMOS logic are connected in parallel with the PMOS transistorsof the latch and form the transmission gates. The fact that the functional blocks are in parallel with the PMOS transistors, the equivalent resistance is smaller during the charging of capacitance [13, 20-22].

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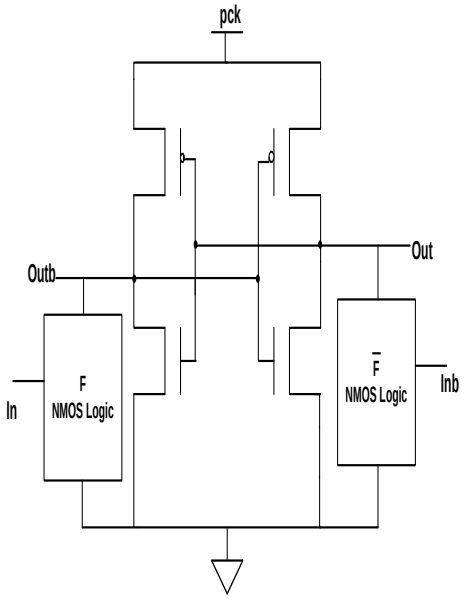

Fig.3: 2N-2N2P Basic Logic circuit

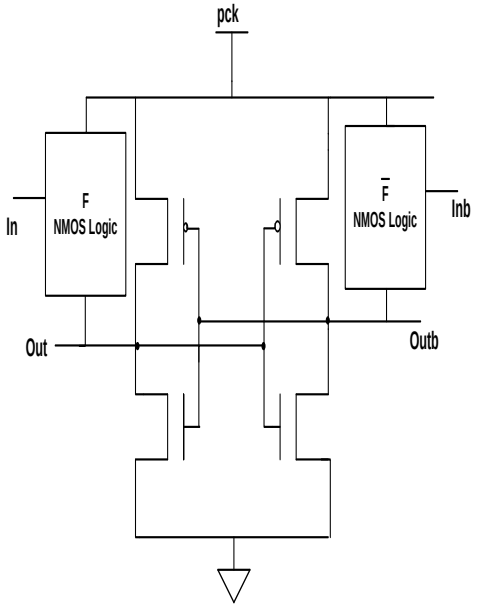

Fig.4: PFAL Basic logic circuit

Assuming input IN High, the device MN3 in F logic block conducts and pulls the OUT node towards power clock CLK, which makes MP2 to switch off and /OUT is disconnected from power clock. This structure provides complete charge recovery by eliminating the charge stored in the output node after the recovery phase. Simulated result in Fig 5 (a) & (b) shown below [23].

We have implemented different logic gates, AND, OR, NAND, NOR, XOR, XNOR using the proposed ON OFF DCDB-PFAL adiabatic logic circuits. Same AC power supply trapezoidal clock is used in the realization of all these circuits. In order to avoid the use of inverters in an adiabatic logic circuit both inputs and outputs are dual rail encoded. Therefore both the positive and negative logic function is available using a single logic circuit.

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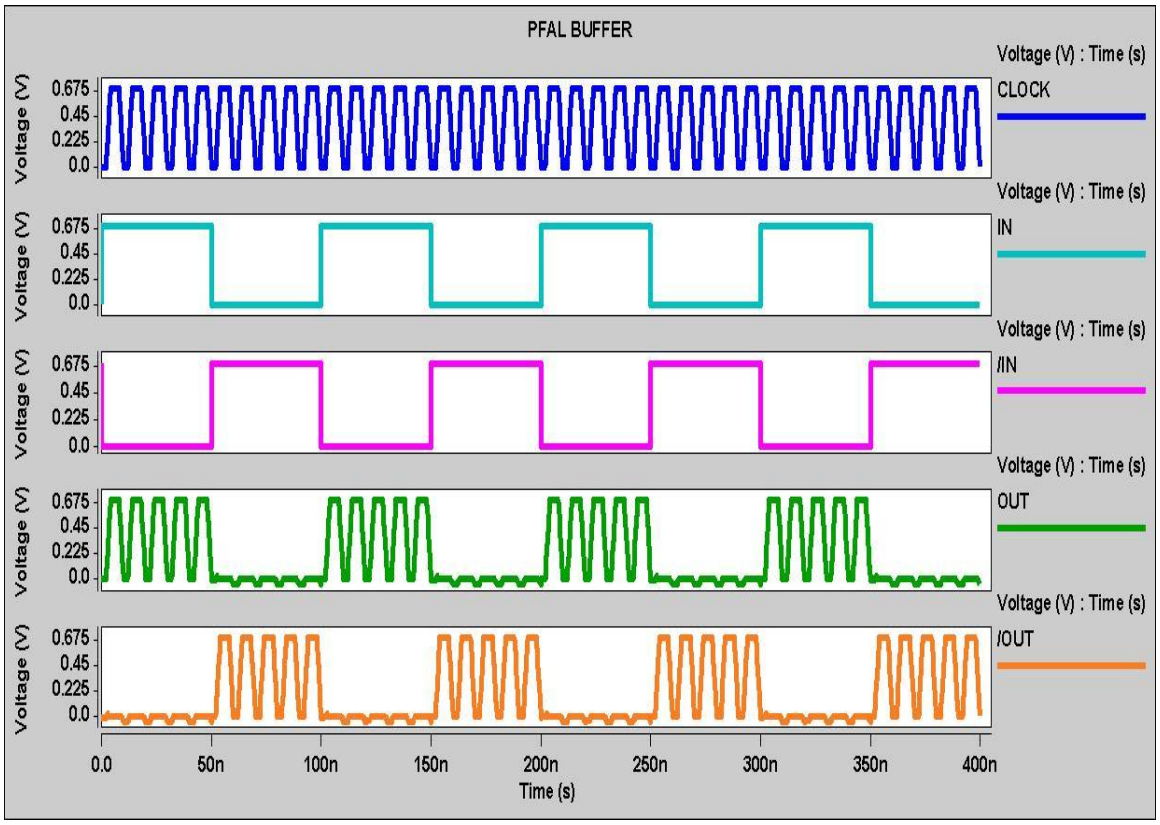

Fig. 5: (a) Basic Structure of Two input PFAL BUFFER Logic (b) Simulated waveform of PFAL BUFFER Logic

SIMULATION AND RESULT

In order to see the effectiveness of different adiabatic logic families over conventional CMOS circuits, different logic gates have been implemented, first using conventional CMOS logic family and then by using the adiabatic principle of different adiabatic logic families as discussed in this paper and power calculations are made as shown in table II.

The universal logic gates have been simulated using PFAL as well as ON OFF DCDB PFAL and the results have been analysed. Fig.6, Shows the comparison of all adiabatic circuit design.

Table. I. Design Parameters

TYPE	CMOS	Adiabatic Logics
PMOS (width)	260 nm	260 nm
NMOS (width)	130 nm	130 nm
Power supply	1 V DC supply voltage	Trapezoidal power clock, 0v- 1v ,frequency: 200MHz
		Rise Time: 1.25 ns, Fall Time: 1.25 ns

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Table II. Average Power Dissipation for Different Logic Devices

LOGIC	GATE	POWER (nW)	DELAY (ps)	PDP (zJ)	EDP E^(-30)
PFAL	INVERTER	0.3432	13.31	4.5680	0.0608
	NOR	0.6828	9.398	6.4170	0.0603
	NAND	0.6553	27.25	17.8569	0.4866
	XNOR	1.241	30.21	37.4906	1.1326
DCDB-PFAL CKT	INV	0.281	12.57	3.5322	0.0035
	NOR	0.5054	8.196	4.1422584	0.0041
	NAND	0.4551	29.43	13.393593	0.0134
	XNOR	0.9634	36.51	35.173734	0.0352

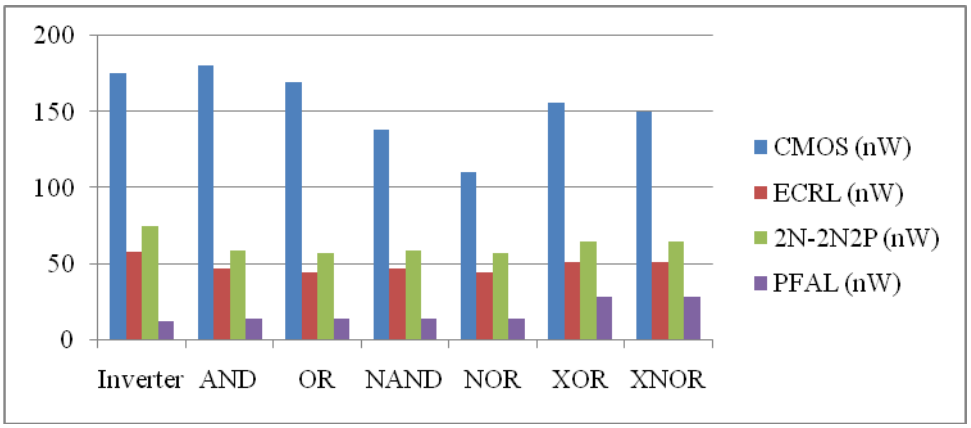

Fig.6: Comparison of Average Power Dissipation for Conventional CMOS and Different Adiabatic Families

CONCLUSION

This paper reviews the adiabatic logic circuits and some important adiabatic logic families have been described and compared for their effectiveness in terms of reduced power dissipation as compared to conventional CMOS logic circuits observed that adiabatic logic designs are quite better than the CMOS logic designs in terms of power consumption which all mostly half than CMOS design by applying trapezoidal pulse saves the power consumption in adiabatic circuit design. The adiabatic logic save the power in dynamic condition mainly it reduces the switching activity of the circuit i.e. there charging and discharging time of the load capacitance is almost reduces, it slowly charge and discharge the transistor. As the quest for ultra-low power circuit designs keeps on increasing, these improved circuit technologies would prove to be very useful in serving the need.The adiabatic logic save the power in dynamic condition mainly it reduces the switching activity of the circuit i.e. there charging and discharging time of the load capacitance is almost reduces, it slowly charge and discharge the transistor.

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