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A NEW TECHNIQUE FOR ULTRA LOW-POWER DESIGN OF DOMINO LOGIC

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Abstract:
As the scaling of technology demand increasing day by day in portable devices such as computers, digital IC, Smart phones, i-pads etc, as a result packaging of the device demand are incorporated in IC with lower consumption for fruitful development of semiconductor. The development of portable devices results in low-power consumption and increase the yield of the circuit. In this paper we proposed different domino logic styles which increases performance compared to existing domino logic styles. According to the simulations in cadence virtuoso 180nm CMOS process, the proposed circuit shows the improvement of up thirty percent compared existing domino logics.

INTRODUCTION

The dynamic logic circuit requires two phases. The first phase, when clock is low, is called the pre-charge phase and the second phase, when clock is high, is called the evaluation phase. In the setup phase, the output is driven high unconditionally (no matter the values of the inputs *A* and *B*). The capacitor, which represents the load capacitance of this gate, becomes charged. Because the transistor at the bottom is turned off, it is impossible for the output to be driven low during this phase.

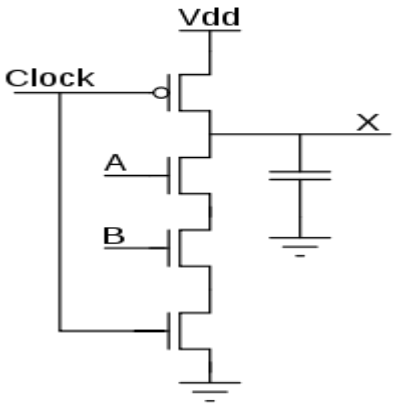

Fig.1 Footed Domino Logic

During the evaluation phase clock is high. If inputs A and B are also high, the output will be pulled low. Otherwise, the output stays high (due to the load capacitance).
Dynamic logic has a few potential problems that static logic does not. For example, if the clock speed is too slow, the output will decay too quickly to be of use. Also, the output is only valid for part of each clock cycle, so the device connected to it must sample it synchronously during the time that it is valid.

DOMINO LOGIC

Domino logic is obtained by adding a static CMOS inverter to the output of basic dynamic CMOS logic. The domino logic gates are non-inverting because of the output inverter. The main idea of building domino logic is to limit charge sharing and charge leakage by feeding back the inverting output, so that we can retain the potential at the dynamic node (the output node of dynamic CMOS logic) with using the charge keeper circuit technique. Dynamic domino logic is typically used for the design of high-speed applications . Unfortunately, the clock distribution network dissipates 45% of the overall consumed power , thus preventing

the use of dynamic domino circuits in low-power applications. Moreover, the distribution of the clock signal involves non-trivial design issues, such as controlling skew and jitter.

Domino CMOS circuit has advantage in terms of high speed and wide fan-in over static CMOS circuits. The domino CMOS circuit suffers from noise margin problem due to charge redistribution between parasitic capacitances at the internal nodes of the circuit and hence false output may be resulted. Domino is non inverting logic with faster switching speed and lesser area as compared to static CMOS logic. Domino logic consists of a single clock, which is used to precharge the dynamic node of the circuit in precharge phase and to evaluate the function made by NMOS network in evaluation phase.

The characteristics are as follows:

- CMOS circuits have no static power dissipation, since the circuits are designed such that the pull-down and pull-up networks are mutually exclusive.
- Low power with high speed – power consumption of CMOS is largely determined by switching power caused by charging and discharging of capacitances. As the circuits get faster, the frequency goes up as does the power consumption.
- Insensitive to device variations- Small size transistors allowed dense layout of circuit although interconnectivity limits the density.
- Rail-to rail swing with $V_{OH} = V_{dd}$ and $V_{OL} = GND$
- Good noise margin- When noise does not exceed the margins, the gate eventually will settle to the correct logic level.
- Robustness against voltage scaling and transistor sizing.
- Number of transistors required to implement an N fan-in gate is 2N. This can results in a significant large implementation area.
- Requires both nMOS and pMOS transistors on each input and pMOS transistors add significant capacitance with relatively large logical effort.
- Suffers from lower performance, especially for large fan-in gates.

2. LITREATURE SURVEY

Basic domino circuits are footed domino logic (FDL) and footless domino logics (FLDL).

High Speed Domino Logic

High speed domino is another domino logic circuit. In domino logic circuit current drawn through the keeper transistor and pull down network NMOS transistors at the beginning of the evaluation phase, can be reduced by applying a clock delay in the circuit. That does not affect the leakage current in the circuit.

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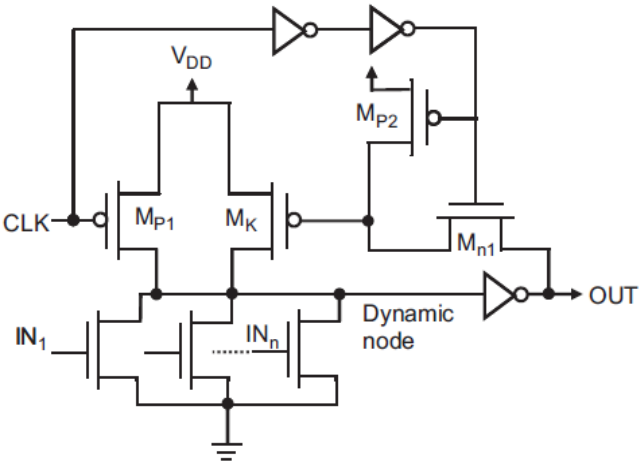

Fig.2. An n-input HS Domino

The architecture of an n-input HS-Domino OR gate is shown in Fig. 2.1. It is similar to Clock Delayed Domino except that the gate O/P is connected to the keeper through an NMOS (M_{n1}) and a PMOS (M_{p2}) device, whose gates are connected to the delayed clock signal.

In High speed domino logic circuit when clock becomes high, M_{n1} is still off and M_{p2} is still on. Therefore M_{p2} turns off the keeper transistor. After some delay of inverter M_{p2} becomes off. Now if dynamic node remains high during the evaluation phase, NMOS is turn on which turns on the keeper transistor. Hence at the beginning of evaluation phase dynamic node is afloat, so in the absence of keeper transistor, evaluation node may be discharged for any noise at the input section. Also the voltage at the gate of the keeper transistor would be V_{DD}-V_{tMn1}. This would provide a dc current flow through the PMOS keeper transistor and the NMOS network.

Split Domino Circuit

The SD gate shown in Fig. 2.2 most of the high speed timing performance schemes, just before or close to the start of the evaluation phase, the input signals of the dynamic logic gates are ready. In such situations the maximum time slot for any output transition is only a fraction of total evaluation time, which takes half time period of 50% duty cycle clock. Therefore at the output of the gate leakage and noise exists for a long time unnecessarily

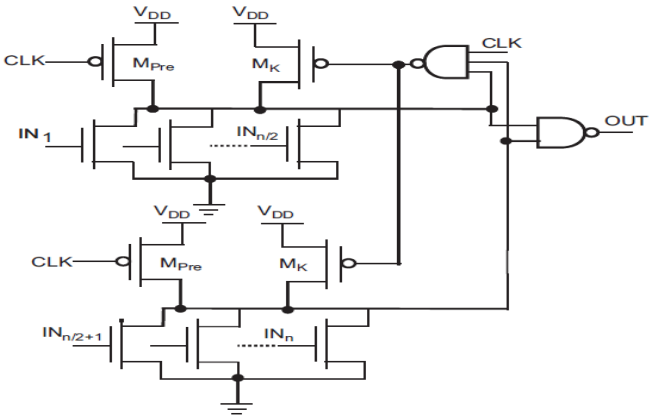

Fig. 3. An n-Input Split Domino OR gate.

The operation of the SD circuit is described as follows: During precharge, CLK is LOW, the keeper devices are OFF and the output is LOW. At the onset of evaluation, the keeper devices remain OFF resulting in minimum contention. There are two different cases that need to be considered during the Evaluation phase.

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decreased dynamic node capacitance and nearly keeps the keeper devices in the OFF state and contention is therefore minimized. The SD keeper is OFF at the onset of evaluation while the conventional keeper is ON. The keeper control signal can be seen to droop and quickly recovers to V_{DD}, maintaining keeper devices virtually OFF.

The overhead of the SD gate represented in the 2-input and 3-input NAND gates results in a slight increase in power dissipation compared to the conventional case.

Single-Phase Sp-Domino

This presents a new limited-switching clock-delayed dynamic circuit technique, called SP-Domino, which achieves static-like switching behaviour, while maintaining the low-area and high-performance characteristics of wide fan-in dynamic gates. SP-Domino is a single-phase footless domino that can be freely mixed with static gates and can provide inverting and non-inverting functions. It is discussed in

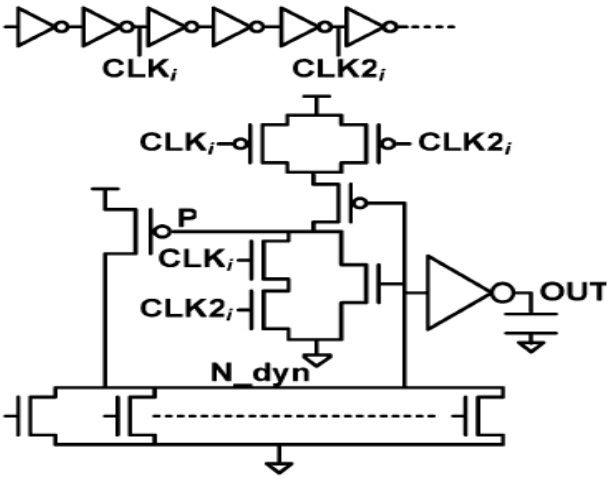

Fig.4. SP Domino Logic

SP-Domino gate is a footless dynamic gate with static input/output characteristics. Its goal is to combine the fast and compact dynamic implementation with the low-switching static behaviour. Unlike a standard domino which is restricted by a low-to-high transition during evaluation, SP-Domino evaluates low-to-high or high-to-low, similar to static gate. Therefore, pre-recharging SP-Domino is actually an evaluation, which leads to single-phase operation. SP-Domino uses a delayed clock for precharge/evaluation, similar to clock-delayed domino, as shown in Fig. 2.3. For a domino gate , its clock is delayed such that the latest arriving input does not arrive later than the rising edge of CLK , which is the major design constraint of an SP-Domino. The gate output can have an evaluation transition (low-to-high) before or right after the rising edge of CLK , whereas it only precharge (high-to-low) right after the rising edge of CLK , after all the domino inputs are available. The next sub-section describes in detail the operation of SP-Domino.

Similar to static gate, the output of SP-Domino gate can stay low or high, transition from low-to-high or from high-to-low during a single clock cycle. The PMOS pull-up in SP-Domino is used as a keeper, as well as a replacement for a static pull-up network. When the pull-down network is held off during a clock cycle,N_dyn is held high due to the feedback keeper, and the output is at state "0." When the pull-down network is held on during a clock cycle, N_dyn is held low and the output is at state "1." However, after the rising edge of CLK, an unconditional path from node P to ground is always created through the two NMOS transistors driven by CLK and its delayed complement $CLK2_i$. This path is kept on for a short time t_{keep} (3 inverters delay). As a result, a small contention period between the keeper and the pull-down network occurs. Short-circuit current flows through this period, but the output and dynamic node do not change their states. This is in contrast to standard domino where the gate evaluates and precharge again when the output should be stable at state "1." When the pull-down network is off and turns on during a clock cycle, a scenario similar to that of a conventional domino gate occurs, and the output transition from low-to-high. When the pull-down network in on and turns off

during a clock cycle, N_dyn node starts charging after the rising edge of CLK_i. The keeper should be sized such that charging N_dyn turns on the feedback nMOS before t_{keep} delay, in order to continue charging N_dyn after the pull-down path created by the clocks is turned off. Charging N_dyn does not suffer from any contention since the SP-Domino pull-down network is off, thus, the keeper can be sized weaker than the pull-down network, in order to allow fast evaluation, while maintaining an equal precharge-evaluation delay. The keeper ratio K is defined as

$$K = \frac{\mu p(\frac{W}{L})keeper}{\mu n(\frac{W}{L})evaluation} \qquad \text{.....(2.3)}$$

where μ_p and μ_n are the holes and electrons mobility, respectively. Notice that beside K, several factors influence the keeper current to evaluation network current ratio, such as threshold voltage. For conventional domino, K provides a way to tradeoff performance and contention power with unity noise gain (UNG). For SP-Domino, the performance is determined by both the pre-charge and evaluation transitions. Therefore, an optimal K exists such that the pre-charge delay equals the evaluation delay, which leads to optimal SP-Domino overall delay. Optimal K is around 0.7. However, the delay increases steeply as K exceeds 0.7. Thus, the keeper ratio should be designed below the optimal delay point to maintain a margin for variations. It can be seen that the input/output behavior of SP-Domino is similar to static gate.

Conventional domino switches two times per cycle when the pull-down network turns on, whereas SP-Domino switches only one time. When the inputs are stable and the output is high, conventional domino keeps evaluating and precharging, whereas SP-Domino nodes are stable. However, SP-Domino still consumes power when the output is stable at state "1" due to the contention current, but this power is much less than the power consumed by the conventional domino.

Current-Comparison Domino

The proposed technique uses the difference and the comparison between the leakage current of the OFF Transistors and the switching current of the ON transistors of the pull down network to control the PMOS keeper transistor,yielding reduction of the contention between keeper transistor and the pull down network from which previously proposed techniques have suffered. Moreover, using the stacking effect, leakage current is reduced and the performance of the current mirror is improved.

In this circuit,the reference current is compared with the pull down network current. If there is no conducting path from the dynamic node to the ground and the only current in the PDN is the leakage current, the keeper transistor will not turn off because the reference current is greater than the leakage current. In fact there is a race between the pull down network and the reference current.The current, which is greater than the other wins the race and turns off its keeper PMOS transistor. Transistor M_{pre2} is removed to discharge node K and thus turning on the keeper transistor in the precharge phase. This results in improved noise immunity. There- fore, unlike circuit designs such as HSdomino in which the keeper transistor is off at the beginning of the evaluation phase,the keeper transistor is on in this design.

The proposed domino circuit is shown in Fig. 2.4. In this circuit M_1 is added in series with the evaluation network such as the wide OR gate, as illustrated in this schematic.

The two phases of the proposed circuit in active mode are explained as follows:

In the precharge phase, clock voltage is in low level (CLK='0' in Fig. 2.4). Hence, transistors M_{pre}, M_{keeper} and M_8 are on and M_1 and M_2 are off. Therefore, the voltage of the dynamic node (Dyn_n) is raised to the high level by transistor M_{pre}.In this phase, the leakage current is decreased due to the stacking effect since the minimum voltage of a MOS transistor in diode configuration is equal to $V_{gs}=V_{ds}=V_{tn}$, where V_{tn} is the NMOS threshold voltage.

In the evaluation phase, clock voltage is in the high level (CLK='1' in Fig. 2.4), so the transistors such as M_{pre} and M_8 are turned off. Depending on inputs levels, the other transistors may be turned on. According to the discharging current of PDN and the mirror current, two states may occur. The gate voltage of the keeper transistor depends upon which current is greater than the other. Then due to the positive feedback consisting of M_4 and M_{keeper} , the voltage of node K is determined.

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First, if all inputs are in low level, the mirror current is greater than the PDN leakage current, the voltage of node K is discharged to zero. Therefore, the keeper transistor is turned on and maintains the dynamic node at a high level.

Second, if at least one input is at a high level, the discharging current of PDN is higher than the mirror current,yielding the voltage of node K to remain high.This reduces the contention problem by turning off the keeper transistor with any great change in the current of the NMOS pull down network rather than the mirror current.

M_2 is a small auxiliary transistor to pull down the footer node (node D in Fig. 2.4) and reduce the delay due to the stacking effect of the NMOS evaluation transistors and M_1. Therefore, the main idea in this circuit is that the keeper transistor is controlled with current comparison so that when the dynamic node is truly discharged, the keeper transistor will be off to prevent the contention current between the keeper and the PDN. Thus, the dynamic power and the propagation delay are reduced. Also, the short-circuit power of the output inverter due to the glitch current is reduced, which relaxes the sizing constraints on the output inverter. As result, when compared to some implementations smaller sized output inverters can be used (from which some techniques suffer). Moreover, leakage power is decreased as a result of the stacking effect.

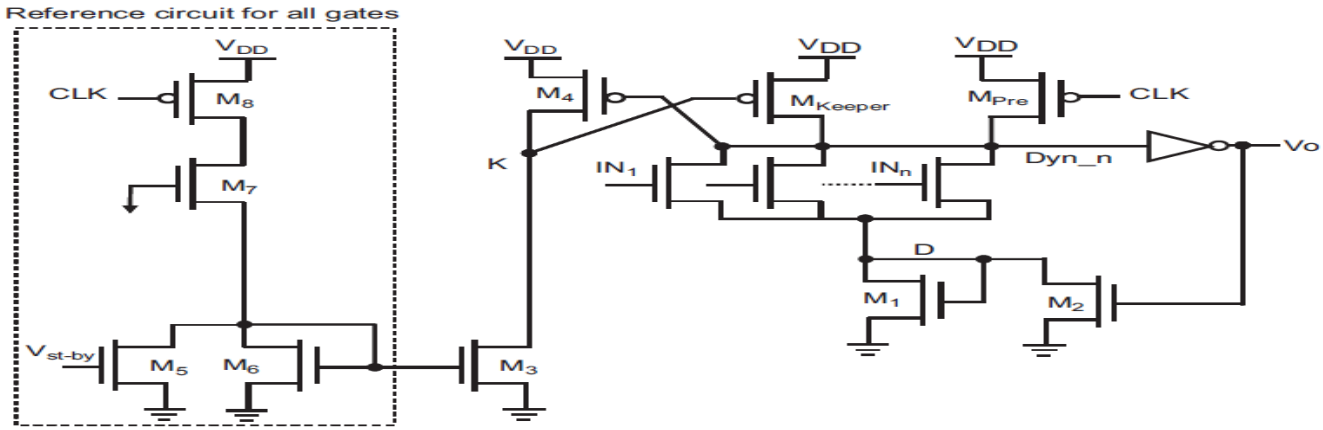

Fig.5. An n-Input Current Comparison Domino OR gate

PROPOSED CIRCUIT

Robustness of domino circuit degrades with the downscaling of the device as leakage power increased. In this report, proposed different domino logic styles which improve the performance and also is capable of providing more than one transition in the evaluation phase and also made possible to provide outputs for precharge phase. To examine the circuit operation a single bit full adder and 4-bit ripple carry adder are developed using proposed design styles. According to the simulations in cadence virtuoso 180nm CMOS process, the proposed circuit shows the improvement of up to 50% compared to conventional domino logic circuits.

A) Level Restorer

When the pull-down network pulls the dynamic node to ground, the pull-up PMOS transistor in the level restorer causes contention, because the effective pull-down current is that of the pull-down network minus the current from the pull-up transistor. Delay is thus increased in this case. This contention can be alleviated by weakening the pull-up transistor, which must be sized such that the voltage at dynamic node is $< 0.1V_{DD}$ when a logic "0" is transmitted by the pull-down network. This condition is fulfilled by decreasing theW/L ratio of the pull-up transistor.

On the other hand, a strong restorer (i.e., with high W/L ratio) is required to achieve sufficient noise margins. A compromise must thus be found between contention and noise margins. Furthermore Furthermore, when increasing the reverse-bias voltage, the reverse ULPD current first increases due to the V_{ds} increase of the transistors. The current reaches a peak value and then strongly decreases as the V_{gs} of the transistors becomes more and more negative. Therefore, this behavior leads to a negative resistance region.

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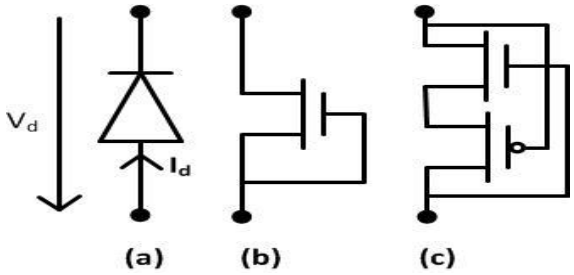

Fig.6. Level restorer

Even though applications using the ULPD operating in a very weak inversion regime, the reverse-biased (i.e.,V < 0) ULPD can also be used in moderate or strong inversion, depending on the threshold voltages of the NMOS and PMOS transistors

used in the diode. Subsequently, higher reverse current peaks in the negative resistance region can be reached for NMOS and PMOS transistors with negative and positive V_t, respectively (depletion-mode NMOS and depletion-mode PMOS transistors). As detailed in the value of this current can be roughly estimated at the intersection of N and P $I_d - V_g$ curves. It is obvious that this high current peak results in a higher leakage current than that of the ULPD operating in the weak inversion regime. However, in order to ensure sufficient level restoration with a short time delay, MOSFETs in depletion mode should be used. The negative resistance region in the ULPD characteristic is exploited here to restore the weak logic level at the sum output node. The ULPD-based level restorers that we used are shown in Fig. 3.4. These depict the low logic-level restorer and the high-logic-level one, respectively. They exploit the potential of MOSFETs in depletion mode with an absolute threshold voltage of 0.25 V. It is also worth noting that such low-doped transistors feature excellent performance in thin-film SOI technology, such as low short-channel effects and parameter variations. low-logic-level restorers are useed in implementation of the circuit that we will describe in next section. C_{node} depicts the input parasitic capacitance, which mainly consists of the drain junction capacitance, at the level restorer node. The operation of the low-logic-level restorer shown in Fig. 3.2(a) is as follows. When the voltage V_{node} is initially set between 0 and V_{dd} /2, the ULPD current I_d is positive and discharges C_{node}. For V_{node} voltages comprised between $V_{dd/2}$ and V_{dd} , both NMOS and PMOS transistors are turned off (since they have negative V_{gs} values). Thus, no current flows through the ULPD. Reciprocally, in the high-logic-level restorer shown in Fig. 3.2(b), when the initial voltage V_{node} lies between $V_{dd}/2$ and V_{dd} , the ULPD current peak drives the voltage V_{node} up to V_{dd}.

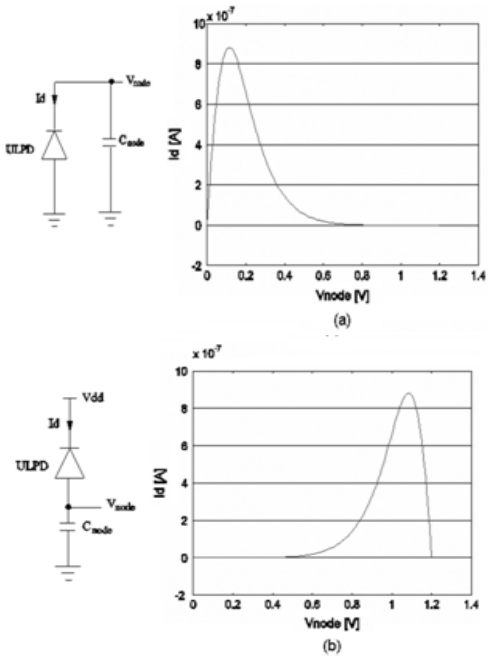

Fig. 7 (a) ULPD based low level restorer and (b) high level restorer

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PROPOSED CIRCUIT :

Proposed circuit uses delayed clock. It uses the function of keeper circuit with slight replacement of the device. The static inverter used here is with low threshold NMOS, turns ON only with the voltage greater than 140mv. High threshold transistor MN4 which turns ON only when the output is strong enough. MN4 used here to prevent further discharge from MN2, and also have to choose MN2 with high threshold.

As usually, in pre-charge phase the dynamic node charges to high. MP2 is in OFF state and the drain terminal of it is at floating, this value passed to keeper transistor. Even in the worst case, if

keeper circuit turns ON, it does not make any difference in operation. At the beginning of pre-charge phase the footer transistor is turned, and it may pull the dynamic node to ground but because of continuing to charge in the pre - charge state, the voltage at the dynamic node remains high.

In the beginning of the evaluation phase, the footer transistor MN1 is in OFF state because of the delay introduced. In this time slot it allows evaluation network to perform its operation. If any input combination tries to pull down the dynamic node, then the voltage difference between dynamic node and footer is very less (in multiples of the threshold voltage of NMOS used in evaluation network), so MN2 transistor turned ON, then the dynamic node pulled down to the ground. This circuitry is used to prevent leakage charge at the beginning of evaluation by utilizing the stacking effect. After delay completion footer transistor turns ON, it makes MN2 to turn OFF.

If no input makes a path between dynamic and footer node, and at the beginning of evaluation phase footer node is at floating state. We have to make sure that this voltage should not turn the MN2 ON, so there is no discharging path for dynamic node to ground at the beginning of the evaluation phase in this case. At this time the output is at a logic low level and makes the keeper transistor MK to serve the dynamic node in charging to its maximum.

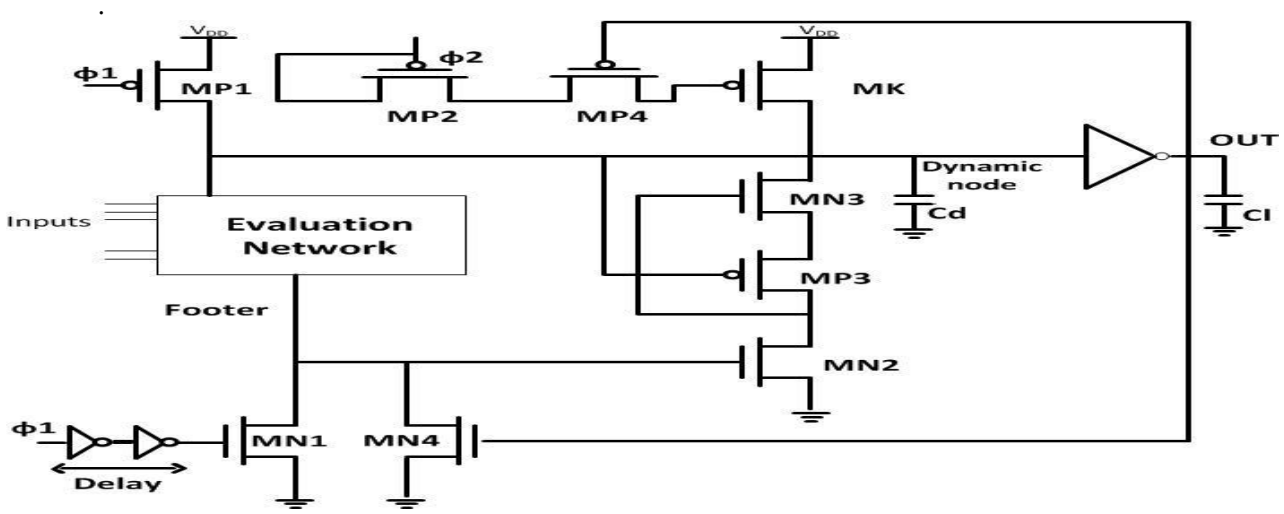

Fig. 8. EVALUATION DOMINO (ED)

Then after, if dynamic node is discharged and if any input disconnected from its operation, at this situation the voltage value of dynamic node is floating, and as mentioned before it turns ON the NMOS transistor and produces a weak low logic level at the inverter output. This low logic turns the MP4 transistor in the linear region. Then a strong low level generated using MP2 and Ø2 in the evaluation phase passed to the keeper transistor MK, which makes MK to switch in saturation state. Transition of dynamic node from 0=>1 made possible in this logic style, and further transitions also takes place in the same manner.

Single phase evaluation

Single clock version of evaluation domino logic is illustrated in Fig.3.4. It avoids the use of dual phase non-overlapping clock generation, but implements the same function

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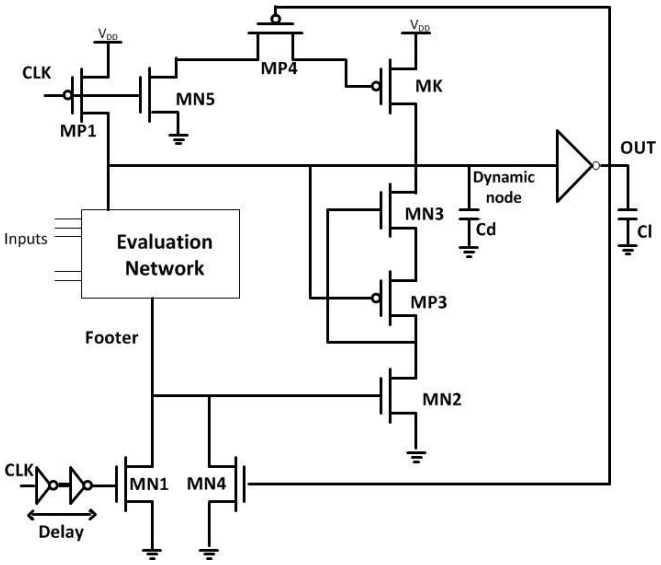

Fig. 9. Proposed static evaluation domino logic(S E D)

Here we just changed in keeper logic generation circuit but the function is same, as mentioned before when the dynamic node is at floating in evaluation phase keeper transistor should be in ON state. The operation of the circuit is carried as before. Using the above circuit logic we can get the fully static output for our inputs, just by modifying the above circuits a little. It can be useful for the improving the performance for the circuit by means of reducing delay and power. We can get the true output even in precharge phase, where as in conventional domino dynamic node could not able to replicate the inputs in precharge phase, as it needed to get charged to V_{DD} irrespective of inputs. In conventional domino logics we are getting outputs according to clock phases i.e we do not expect any output other than logic low in precharge phase but in case of high fan-in gates or high frequency inputs every transition in the inputs are needed to be mirrored at he output, where conventional domino logic circuits are failing and irrespective of inputs dynamic node to be charged and discharged, even though there is no transitions in input signals. This leads to increament of power dissipation because of increased switching power dissipation caused by clock following dynamic node.

By modifying the proposed circuit a little I could able to build the fully static domino circuit. Power can be decreased in this logic because we are avoiding unnecessary switching power dissipation. In conventional domino circuits we need to wait for the next evaluation phase to get output for our input signal if there is any transition in inputs in precharge phase, where as in fully static domino logic style we are getting output instantly with a negligible delay in static manner, so the delay can be reduced by using this static domino style. We can get the over all improved power delay product as aresult as well.

RESULTS

All the existing and proposed circuit is simulation to obtain the high performance without degradation of Noise immunity of the circuit. Here we have calculate the leakage power in evaluation network (Wide OR Gate) and calculate the leakage power consumption by calculating the UNG of the circuit, active mode power consumption A.C noise margin of the proposed designed topologies and the comparisons have also been made with the reported circuits by performing simulation on Cadence Virtuoso software using 90nm and 65nm CMOS technology. Some parameters of the proposed circuit such as delay, average power, unity noise gain are calculated (Table II) for 8 input OR gate. In the proposed circuit we find improvement in these parameters as compare to the previous domino logic circuit. The comparison of unity noise gain of the proposed circuit with other standard domino logic circuit is shown in table II and III. Table III shows the comparison of 16 input OR gate proposed circuit with footed domino logic circuit, footless domino logic circuit, high speed etc. domino logic circuit. The circuit is simulated at 65nm technology in cadence spectre at 1V. For 8 and 16 input fan in OR gate comparison between well known existing circuit design techniques, we performed several simulations to obtain UNG and dissipated power as shown in the table.

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TABLE .1 Power, Delay and PDP Comparison of Reported and Proposed domino circuits.

Topology	FLDL [11]	FDL [11]	HSDL [5]	CKL [6]					**Proposed**
					`	ED	SED	FCD	FED
Power dissipation(µw)	10.4	8.27	6.58	11.1		5.31	5.28	4.32	4.17
Delay(ns)	0.396	0.44	0.404	0.41		0.240	0.24	0.18	0.18
PDP(fJ)	4.11	3.62	2.65	4.58		1.27	1.26	0.77	0.75

TABLE .2: COMPARISION OF POWER DESSIPATION (in µW)

S. No.	LOGIC STYLE	8 INPUT		16 INPUT		32 INPUT	
		65nm	90nm	65nm	90nm	65nm	90nm
1.	SFLD	7.200	18.84	9.586	14.01	12.33	16.29
2.	FLD	8.227	13.44	14.00	22.97	17.04	23.83
3.	HSD	494.1	835.5	495.6	4220	5633	5762
4.	CKD	264.5	496.6	266.8	499.4	298.3	301.2
5.	WFD	8.908	13.69	14.30	14.30	19.38	27.91
6.	LCR	6.039	9.015	8.210	11.85	12.39	15.27
7.	CCD	6.125	11.75	14.86	16.93	19.34	26.20
8.	Proposed Circuit	2.793	4.239	4.376	6.945	7.021	9.023

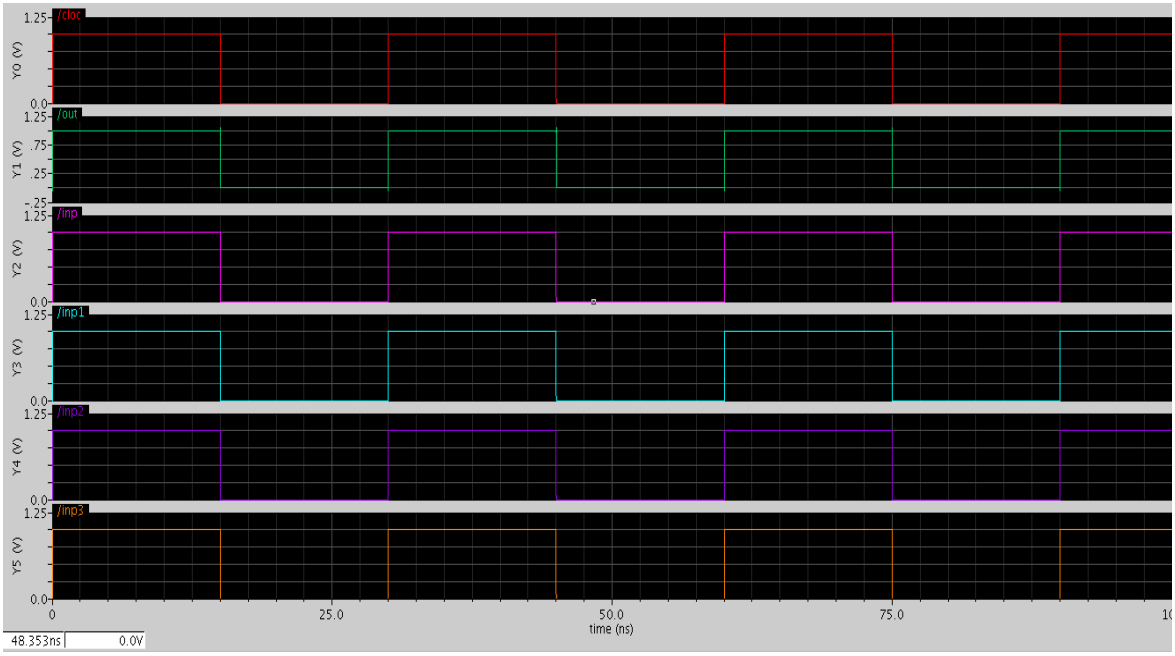

Fig. 9. Output wave form for proposed Fully static clocked domino logic

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As it can be seen propsed logic design shows significant improvement in performance. Table1 shows the results at vdd =1.2 for CL=100fF. Delay time for proposed circuit is reduced because we are using separate path to discharge, makes it quickly discharge at the beginning of evaluation phase. Leakage power is reduced by introducing stacking effect.

The output wave forms are illustrated in Fig. 4.1 As mentioned before proposed static evaluation circuit can capable of providing true output in evaluation phase and proposed fully static clocked domino logic able to provide static output irrespective of clock (phase). Area comparison of different domino logic styles are reported. Number of devices in topology, device size and optimization of device sizes are considered.

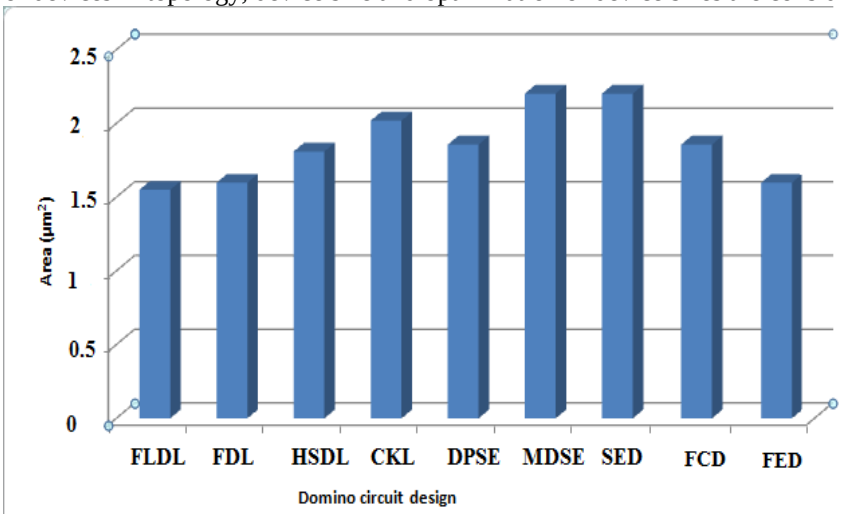

Fig. 10. Area comparison for proposed topologies with reported domino topologies

TABLE.3: COMPARISION OF UNG

S. No.	LOGIC STYLE	8 INPUT		16 INPUT		32 INPUT	
		65nm	90nm	65nm	90nm	65nm	90nm
1.	SFLD	0.2984	0.312	0.272	0.289	0.253	0.273
2.	FLD	0.3273	0.349	0.316	0.324	0.302	0.316
3.	HSD	0.2962	0.314	0.277	0.293	0.256	0.267
4.	CKD	0.3079	0.328	0.279	0.293	0.249	0.267
5.	WFD	0.3293	0.346	0.317	0.324	0.302	0.317
6.	LCR	0.3441	0.365	0.323	0.337	0.309	0.324
7.	CCD	0.3572	0.389	0.339	0.356	0.314	0.336
8.	Proposed Circuit	03821	0.421	0.367	0.382	0.346	0.268

Conclusion

To enhance the performance of the domino logic style, we added three extra footer transistors and applied semi-domino logic style to come up with proposed logic style. This semi-domino logic style decreases switching at the output node; this facilitates reduction of power consumption of the circuit. Furthermore, the circuit becomes noise robust. The 3 extra footer transistors enhance the operational speed of the new domino logic which leads to decrease the delay of the circuit. Through extensive simulations the above ideas regarding speed, power and noise were validated. This proposed logic style has been

compared with all basic domino logic styles and also some previous proposed logic styles in the same environment.. It is observed when we used a high frequency inputs. Also our proposed domino circuits have more number of transistors and , our proposed multipliers suffer from complex design. Finally, it has been

examined that the proposed circuits have optimum performance in terms of power dissipation,delay and output reliability. All simulation are done using CADENCE UMC environment.

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